CLAIMS

What is claimed is:

1. An apparatus comprising:

an idle removal block operating at a first clock speed to remove idles from received data packets;

a buffer coupled to the idle removal block to receive the data packets from the idle removal block, the buffer generating an idle insertion control signal to the idle removal block to enable the removal of idles by the idle removal block;

an idle insertion block operating at a second clock speed coupled to the buffer to receive data packets from the buffer and insert idles into the data packets, the idle insertion block receiving an idle insertion control signal from the buffer to enable the insertion of idles.

2. The apparatus of Claim 1 wherein the buffer comprises a dual port memory, wherein the idle removal block is coupled to one port of the dual port memory and wherein the idle removal block is coupled to the other port of the dual port memory.

3. The apparatus of Claim 1 wherein the buffer comprises write control logic for writing packets from the idle removal block into the buffer and wherein the write control logic generates the idle insertion control signal based on the write capacity of the buffer.

4. The apparatus of Claim 3 wherein the write capacity includes the memory currently available to the write control logic for writing packets into the buffer.

5. The apparatus of Claim 1 wherein the buffer comprises read control logic for reading packets from the buffer and wherein the read control logic generates the idle removal control signal based on the read capacity of the buffer.

6. The apparatus of Claim 5 wherein the read capacity includes the memory currently filled for the read control logic to read packets from the buffer.

7. The apparatus of Claim 1 wherein the buffer receives the data packets from the idle removal block based on the first clock frequency, and wherein the idle insertion block receives data packets from the buffer at the second clock frequency.

8. An apparatus comprising:

means, operating at a first clock speed, for removing idles from received data packets;

means for buffering data packets coupled to the means for removing for receiving the data packets from the means for removing, the means for buffering generating an idle insertion control signal to the means for removing to enable the removal of idles by the means for removing;

means, operating at a second clock speed, coupled to the means for buffering for receiving data packets from the means for buffering and for inserting idles into the data packets, the means for inserting receiving an idle insertion control signal from the means for buffering to enable the insertion of idles.

9. The apparatus of Claim 8 wherein the means for buffering comprises a dual port memory, wherein the means for removing is coupled to one port of the dual port memory and wherein the means for removing is coupled to the other port of the dual port memory.

10. The apparatus of Claim 8 wherein the means for buffering comprises means for writing packets from the means for removing into the means for buffering and wherein the means for writing generates the idle insertion control signal based on the write capacity of the means for buffering.

11. The apparatus of Claim 8 wherein the write capacity includes the memory currently available to the means for writing for writing packets into the means for buffering.

12. The apparatus of Claim 8 wherein the means for buffering comprises means for reading packets from the buffer and wherein the means for reading generates the idle removal control signal based on the read capacity of the means for buffering

13. The apparatus of Claim 8 wherein the read capacity includes the memory currently filled for the means for reading to read packets from the means for buffering.

14. The apparatus of Claim 8 wherein the means for buffering receives the data packets from the means for removing based on the first clock frequency, and wherein the means for inserting receives data packets from the means for buffering at the second clock frequency.

15. A method comprising:

receiving a data packet;

detecting a buffer capacity relative to the packet;

removing idles from the packet depending on the detected buffer capacity;

writing the packet into the buffer at a first clock rate and;

reading the packet from the buffer at a second clock rate.

16. The method of Claim 15, further comprising halting the writing of the packet during removing idles.

17. The method of Claim 15 further comprising inserting idles into the packet after reading the packet to create a second packet at the second clock rate.

18. The method of Claim 15, further comprising halting the reading of the packet during inserting idles.

19. The method of Claim 15, further comprising generating an error signal if the buffer capacity is exceeded.

20. The method of Claim 15 wherein detecting a buffer capacity relative to the packet comprises determining the memory currently available for writing packets into the buffer.